

(19)



JAPANESE PATENT OFFICE

## PATENT ABSTRACTS OF JAPAN

(11) Publication number: **05266657 A**(43) Date of publication of application: **15.10.93**

(51) Int. Cl.

**G11C 11/406**(21) Application number: **04064432**(71) Applicant: **NEC CORP**(22) Date of filing: **23.03.92**(72) Inventor: **MUROTANI KITOKU**(54) **DYNAMIC SEMICONDUCTOR MEMORY**

## (57) Abstract:

**PURPOSE:** To reduce the power consumption of the dynamic semiconductor memory in its refresh operation.

**CONSTITUTION:** A memory cell array is divided into a plurality of memory cell arrays 9a, 9b, column decoders 7a, 7b, word drive circuits 8a, 8b and sense amplification circuits 11a, 11b are arranged respectively at the memory cell arrays 9a, 9b. Control signals  $\phi a$ ,  $\phi b$  for executing a refresh operation which is matched to a memory cell at the minimum data holding time of the individual memory cell arrays 9a, 9b are generated by using an internal control-signal generation circuit 3. Thereby, the memory cell arrays 9a, 9b are refreshed.

COPYRIGHT: (C)1993,JPO&amp;Japio

